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NNJ-TPLLV1/A

Quick start user guide

REV. H

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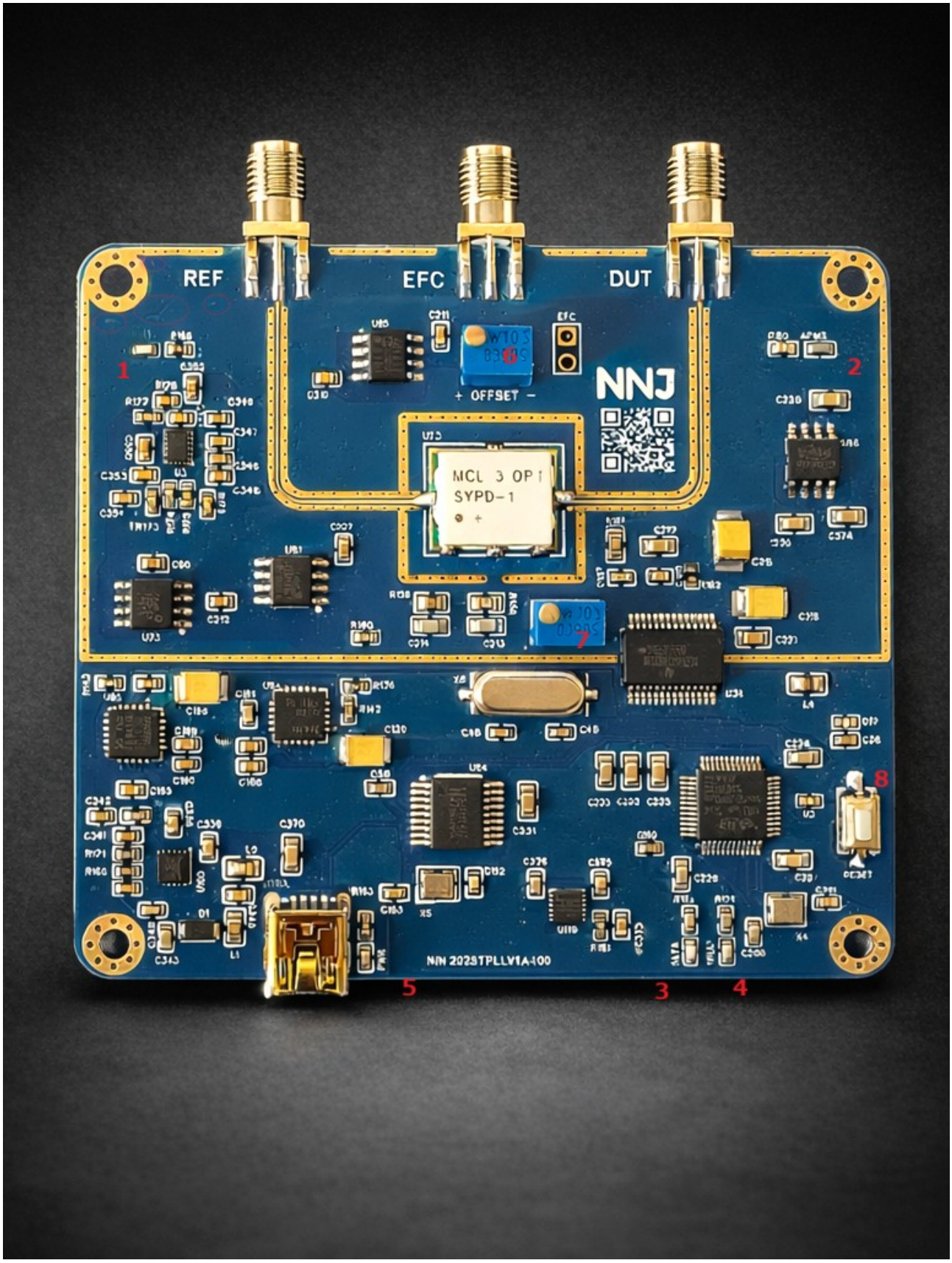

REF
EFC
DUT
1
2
3
4
5
6
7
8
+ OFFSET −
NNJ
MCL 3 OP
SYPD-1
NNJ 2023TPLLV1A100

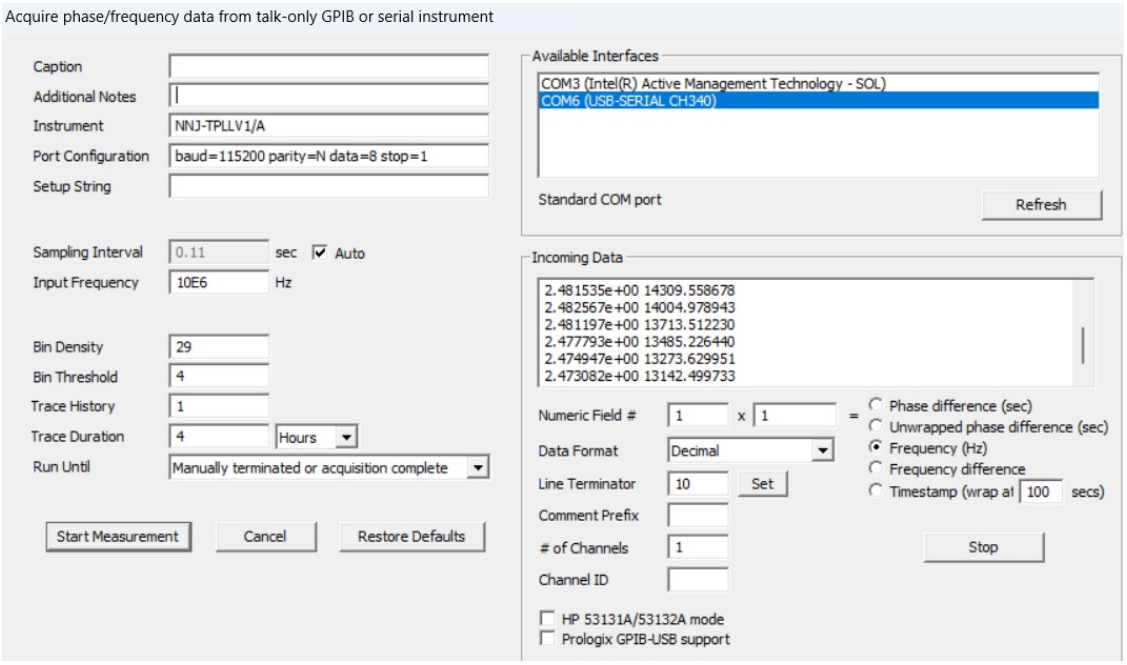
- **1. PLL STATUS LED**
- **2. ANALOGUE POWER STATUS LED**
- **3. DATA STREAM STATUS LED**
- **4. TIGHT PLL STATUS LED**
- **5. DIGITAL POWER STATUS LED**
- **6. OFFSET CONTROL**
- **7. GAIN CONTROL**
- **8. RESET BUTTON**

UART CONNECTION : BAUD RATE 115200 , 8,1,N – APPEAR AS CH340
DATA RATE (FIXED) : 0.1 SECOND
EFC OUTPUT : MAX +/- 3.5 V

EXAMPLE OUTPUT :

1.790728e+00 -3359.046173
1.783133e+00 -3453.221512
1.791057e+00 -3301.825714
1.791064e+00 -3484.215927
1.777067e+00 -3485.408020
1.776427e+00 -3561.105919
1.776253e+00 -3513.422203
1.770705e+00 -3637.399864
1.763964e+00 -3694.620323

In Timelab , open as Acquire → Counter in Talk-Only mode. Example screen below for 10 MHz:



Q&A

1. I want to measure the noise floor of the board. Can I simply split a reference signal to both REF and DUT without using the EFC?

No.

To properly measure the residual noise floor, the loop must be closed. The ADC and MCU calculations are not part of the active PLL loop itself. Therefore, measuring with the loop open will not reveal the true residual performance.

To evaluate the residual floor correctly, you must:

- Lock two sources together via the EFC pin (closed-loop condition).
- Split the signals.
- Measure them using a TIC or a TSC-like instrument, especially to observe short τ (tau) behaviour.

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2. How can I maneuver the (T)PLL?

The first column in the data stream represents frequency using an arbitrary 1 Hz/V scale. However, it is also directly proportional to the buffered output voltage of the first-stage amplifier feeding the ADC (this corresponds to LED No. 1 in the manual).

The second column represents the phase detector IF output voltage in microvolts (µV). This is a differential measurement taken before the double low-pass filter.

Practical Example

Suppose two Vectron OCXOs are connected to REF and DUT, with the EFC connected to REF. By first adjusting the offset (the upper trimmer) and then slightly adjusting the gain, the following data stream may be obtained:

```
2.665919e+00 236.902046
2.665863e+00 250.611115
2.666429e+00 243.458557
2.665918e+00 244.650650
2.666081e+00 404.391098
```

At this point, the loop is closed.

There are two test pads near the EFC trimmer:

- Measuring with a multimeter shows the EFC voltage is approximately 0.5 V.
- The ADC level (first column) is approximately 2.6 V.
- The SYPD1 output (second column) is near zero, around 200 µV.

In general, when the second column remains within ±5000 µV, the TPLL indicator (LED No. 4, the lower LED near the data output) will illuminate. This provides visual confirmation that the system is entering the tight phase-lock region.

The other PLL indicator (LED No. 1) is also helpful when locking two sources, as it directly reflects the first-stage output level. You may experiment by connecting two separate OCXOs without EFC to observe the behavior.

Optimal Operating Point

The optimal operating point is not fixed — it strongly depends on the OCXOs under test.

Based on experience with commercially available units, the ADC input typically settles between 2.6 V and 2.9 V (first column) under optimal conditions.

Offset and Gain Adjustment

The Bourns trimmer adjustment knobs are small. Please use an appropriately sized flat screwdriver and handle them carefully.

These controls are meant to be actively adjusted — they are essentially your “rudder” for locking the sources. There is no need to worry about the initial calibration.

One important reference point:

The DC offset removal implemented in the MCU is designed for 10 MHz operation (as specified in the SYPD1+ datasheet). If you operate at other frequencies, post-processing adjustments may be required.

The mechanical limits of the trimmers are easy to identify — you will hear a slight “click” at the end of their rotation range.

It is generally easier to:

1. Open a terminal program (e.g., PuTTY) while making adjustments.
2. Close it.
3. Then open TimeLab when you are ready to begin sampling.

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3. What are the correct topologies for using the TPLLV1/A in MODE A and MODE B?

MODE A

→ Two identical sources (e.g., two 10 MHz OCXOs)
→ EFC connected to REF

MODE B

→ DUT is the most stable reference source (for example, a Rubidium or GPS standard).
→ REF is the follower that will be locked to the DUT.
→ EFC is connected to REF in this case as well.

Adjust offset and gain according to the desired locking behavior.

4. I successfully locked my OCXO to a GPSDO and to a Rubidium using MODE B, but the output from the TPLLV1/A does not represent the true ADEV of the GPSDO, even though the signals appear perfectly locked on the oscilloscope. Why?

In **MODE B**, the unit operates as an active **servo loop**. The output therefore reflects the **EFC (Electronic Frequency Control) variations**, which represent the effort of the PLL to maintain lock between the oscillators.

For this reason, the output does **not represent the true Allan deviation of the locked sources**.

The **TPLLV1/A output should only be used in MODE A** for direct phase/frequency measurements.

To properly monitor the performance of the lock in MODE B, the oscillator outputs should be **split and measured with an external instrument**, such as a **TIC, DMTD system, or TSC**, referenced to a highly stable frequency standard.